**AKSHEYAA COLLEGE OF ENGINEERING**
Puludivakkam, (Near Nelvoy Junction), Maduranthagam Taluk,
Kancheepuram 603 314, Tamil Nadu, India.
Phone: + 91 44 27568004-02-05, email: principal@ace.ac.in
**(An ISO 9001:2008 Certified Institution)**

## DEPARTMENT OF SCIENCE & HUMANITIES

**Branch: CSE** **I Year / II Semester**

**Subject Code / Name: CS6201/ DIGITAL PRINCIPLES & SYSTEM DESIGN**

## UNIVERSITY QUESTIONS
## PART-A

### *UNIT -1*
### *BOOLEAN ALGEBRA AND LOGIC CIRUIT*

**1)** Convert (0.6875) to binary. **(May-15)**
**2)** Prove the following using DeMorgan's theorem. ((x+y)'+(x+y)')'=x+y. **(May-15)**
**3)** Find the octal equivalent of hexadecimal number ABCD. **(May -14)**
**4)** State and prove the consensus theorem. **(May-14)**
**5)** State the principle of duality. **(Nov-14)**
**6)** Implement AND gate using only NOR gates. **(Nov-14)**
**7)** Convert 231.3 to binary. **(May-14)**
**8)** Simplify Z = (AB+C)(B'D+C'E')+(AB+C)'. **(May-14)**
**9)** Realize G = AB'C+DE+F' using NAND gates. **(May-14)**
**10)** Convert $(1001010.1101001)_2$ to base 16 and $(231.07)_8$ to base 10. **(Nov-13)**
**11)** Realize XOR gate using only 4 NAND gates. **(Nov-13)**
**12)** Convert $(101101.1101)_2$ to decimal and hexadecimal form. **(May-13)**
**13)** What are the limitations of Karnaugh Map? **(May-13)**
**14)** Find the complement and dual of F = (y'z'+yz). **(Nov-12)**
**15)** Realize OR gate using only NAND gates. **(Nov-12,05)**
**16)** Write the applications of Gray code? **(May-12)**
**17)** Perform the following code conversion. $(1010.10)_2=(?)_{16}\rightarrow(?)_8\rightarrow(?)_{10}$ . **(Nov-11)**
**18)** State the different ways for representing the signed binary numbers**.** **(Nov-11)**
**19)** Simplify the expression ((AB'+ABC)'+A(B+AB'))'. **(Nov-11)**
**20)** Write the truth table of logical AND and XOR gates. **(May-11)**
**21)** Represent the decimal numbers -200 and 200 using 2's complement binary form. **(May-11)**
**22)** State and prove Consensus theorem. **(Nov-10)**
**23)** Find the octal equivalent of hexadecimal number. $(AB.CD)_H$ . **(Nov-10)**
**24)** Simplify the following Boolean functions to a minimum number of literals.
(a) (x+y)(x+y') (b) xy+x'z+xz **(May-10,07, Nov-08)**
**25)** Convert the $(153.513)_{10}$ to octal. **(May-10)**

**26)** State the duality principle. **(May-10)**
**27)** Draw the logic diagram for the Boolean expression ((A+B)C)'D using NAND gates**.** **(Nov-09)**
**28)** Simplify the following Boolean function by K-map. F(A,B,C,D) = Σm (1,5,9,12,13,15). **(May-15)**
**29)** Simplify the following Boolean expression to a minimum number of literals. AB+ACD+ABD+ABCD. **(May-09)**
**30)** Show that A+A'B=A+B using the theorems of Boolean Algebra. **(Nov-05)**
**31)** Convert $(126)_{10}$ to octal number & Binary number. **(Nov-15)**
**32)** Write short notes on Weighted Binary codes. **(Nov-15)**

## *UNIT – II*
## *COMBINATIONAL LOGIC*

**33)** Discuss NOR operation with a truth table. **(Nov-15)**
**34)** Draw the truth table of Half adder. **(Nov-15)**
**35)** Implement a full adder with 4×1 Multiplexer. **(May-15)**
**36)** Write the Data flow description of a 4-bit comparator. **(May-15)**
**37)** Implement the following Boolean function using 4:1 MUX F(A,B,C)=ΣM(1,3,5,6). **(Nov-14)**
**38)** Implement the function G = Σm (0,3) using a 2×4 decoder. **(May-14)**
**39)** Draw the circuit of 2 to 1 line multiplexer. **(May-14)**
**40)** Realize 4-bit binary to gray code converter using EX-OR gates. **(May-14)**
**41)** State the difference between demultiplexer and decoder. **(May-14)**
**42)** Obtain the truth table for BCD to Excess-3 converter. **(Nov-13)**
**43)** Draw the truth table and circuit diagram of 4 to 2 Encoder. **(Nov-13)**
**44)** Wrote down the truth table of a full subtractor. **(May-13)**
**45)** Distinguish between a decoder and a Multiplexer. **(May-13)**
**46)** Implement a 4-bit even parity checker. **(Nov-12)**
**47)** Construct a 4×16 decoder using 3×8 decoders. **(Nov-12)**
**48)** With block diagram, show how a full adder can be designed by using two half adders and one OR gate. **(Nov-11)**
**49)** Implement a full adder with two half adders. **(Nov-12)**
**50)** List the modeling techniques available in HDL. **(Nov-11, May-07)**
**51)** Define decoder. Draw the block diagram and truth table for 2 to 4 decoder. **(Nov-11)**
**52)** Define logic synthesis and simulation. **(May-12)**
**53)** Draw the schematic of half adder logic. **(May-11)**
**54)** Determine the number and size of multiplexers required to implement a full adder. **(May-11)**
**55)** Compare the serial and parallel adder. **(Nov-10)**
**56)** Define Look ahead carry adder. **(Nov-10)**
**57)** Define priority encoder. **(Nov-10)**
**58)** Write a dataflow description of a 2 to 1 MUX. **(Nov-10)**
**59)** Obtain the Boolean functions for the output of the half subtractor. **(May-10)**
**60)** Write the Boolean function for 3-bit even parity generator and draw the circuit. **(May-10)**
**61)** What is an encoder? List its applications. **(May-10)**

**62)** Compare a decoder with a demultiplexer**.** **(May-10)**
**63)** Draw the logic diagram for half adder. **(Nov-09)**
**64)** What is the difference between decoder and demultiplexer. **(Nov-09)**
**65)** Write down the difference between sequential and combinational circuit. **(Nov-09, May-10)**
**66)** Give some applications of multiplexers**.** **(May-09)**
**67)** What is the need for code conversion? Give two commonly used codes. **(May-09)**

## *UNIT – III*
## *SYNCHRONOUS SEQUENTIAL LOGIC*

**68)** Draw the diagram of T flip flop and discuss its working. **(Nov-15)**
**69)** What is a shift register? **(Nov-15)**
**70)** Give the block diagram of Master –Slave D flip flop. **(May-15)**
**71)** What is a Ring counter? **(May-15)**
**72)** Distinguish Mealy and Moore circuit. **(Nov-14,10)**
**73)** With reference to a JK flip flop, what is racing? **(Nov-14)**
**74)** Write the characteristics table and equation of JK flip flop. (**May-14)**
**75)** Write any two applications of shift register. **(May-14, Nov-10)**
**76)** Write the HDL code to realize a D flip flop. **(May-14)**
**77)** Realize a JKFF using DFF and gates. **(Nov-13)**
**78)** Write HDL code for up-down counter suing behavioral model. **(Nov-13)**
**79)** Derive the characteristics equation of a JKFF. (**May-13)**
**80)** What is a Mealy circuit? **(May-13)**
**81)** List any two mechanisms to achieve edge triggering of flip flops. **(Nov-12)**
**82)** What is a ring counter? **(Nov-12)**
**83)** How many flip flops are required for designing synchronous MOD 60 counter? **(Nov-11)**
**84)** Write down the characteristics equation for JK and T flip flops. **(Nov-11)**
**85)** Write the state transition table of JKFF. **(May-11)**
**86)** Express the next state characteristics of D and SR flip flops. **(May-11)**
**87)** What is the idea behind master slave JKFF? **(May-10)**

## *UNIT – IV*
## *ASYNCHRONOUS SEQUENTIAL CIRCUIT*

**88)** What is race condition? **(Nov-15, May-14, Nov-11,09)**
**89)** Compare synchronous and asynchronous sequential circuit. **(May-15)**
**90)** What is a critical race condition? Give example. **(May-15, Nov-10)**
**91)** Define Hazard. **(Nov-14, Nov-11)**
**92)** How many states are there in a 3-bit ring counter? What are they**?** **(Nov-14)**
**93)** What are the types of hazards? **(May-14, Nov-11,Nov-10)**
**94)** State the rules for state assignment**.** **(May-14)**

**95)** What are cycles and races? **(May-14)**
**96)** Define primitive flow table. **(Nov-13, May-13)**
**97)** What are static'1' hazard and static'0' hazard? **(May-13)**
**98)** Draw the block diagram of an asynchronous sequential circuit. **(Nov-12)**
**99)** Define static and dynamic hazards. **(May-11)**
**100)** Is it essential to have race free assignment? Justify**.** **(May-10)**
**101)** Does race condition exist in synchronous or asynchronous sequential circuit? Why? **(May-10)**
**102)** What are the steps for design of asynchronous sequential circuit? **(Nov-09)**

## *UNIT – V*
## *MEMORY AND PROGRAMMABLE LOGIC*

**103)** What is a memory address register? **(Nov-15)**
**104)** Write short notes on PLA. **(Nov-15)**
**105)** Differentiate between EEPROM and PROM**.** **(May-15)**
**106)** How to detect double error and correct single error? **(May-15)**
**107)** Whether PAL is same as PLA? Explain. **(Nov-14)**
**108)** What is a volatile memory? Give example. **(Nov-14)**
**109)** What is memory decoding? **(May-14)**
**110)** Define ASIC. **(May-14)**
**111)** State the difference between PAL and PLA. **(May-14, Nov-11)**
**112)** Distinguish EEPROM and flash memory**.** **(Nov-13)**
**113)** Compare SRAM and DRAM. **(May-13)**
**114)** Determine the number of address lines required for 512 bytes of memory and for a 2KB memory. **(May-11)**
**115)** What is programmable logic array? How does it differ from ROM? **(Nov-09)**

## PART-B

### *UNIT -1*
### *BOOLEAN ALGEBRA AND LOGIC CIRUIT*

**NOV/DEC 2015**

**1)** Simplify the following switching functions using Karnaugh map method and realize expression using gates $F(A,B,C,D) = \Sigma(0, 3, 5, 7, 8, 9, 10, 12, 15)$. **(16marks)**

**2)** Simplify the following switching functions using Quine McCluskey's tabulation method and realize expression using gates $F(A,B,C,D) = \Sigma(0, 5, 7, 8, 9, 10, 11, 14, 15)$**.** **(16marks)**

**APRIL/MAY 2015**

**1)** Simplify the following Boolean expression in (i) sum of product (ii) product of sum using K-map. F= AC'+B'D+A'CD+ABCD**.** **(16marks)**

**2)** Express the following function in sum of minterms and product of maxterms F(x,y,z)=x+yz. **(8marks)**

**NOV/DEC 2014**

**1)** Simplify the following $F(w,x,y,z)=\Sigma m(2, 3, 12, 13, 14, 15)$, using tabulation method. Implement the simplified function using gates. **(16marks)**

**2)** Simplify the Boolean function in sum of products (SOP) and product of sums (POS). $F(A,B,C,D)=\Sigma m(0, 1, 2, 5, 8, 9, 10)$. **(10marks)**

**3)** Plot the following Boolean function in K-map and simplify it. $F(w,x,y,z)=\Sigma m(0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14)$. **(6marks)**

**APRIL/MAY 2014**

**1)** Simplify the following functions using k-map techniques. (i) $G = \pi M(0, 1, 3, 7, 9, 11)$ (ii) $f(w,x,y,z) = \Sigma m (0, 7, 8, 9, 10, 12) + \Sigma d (2, 5, 13)$. **(16marks)**

**2)** Minimize the expression using Quine McCluskey (Tabulation) method. $F = \Sigma m(0, 1, 9, 15, 24, 29, 30) + \Sigma d (8, 11, 31)$. **(16marks)**

**3)** Add, Subtract and Multiply the following numbers in binary 110010 and 11101. **(6marks)**

**4)** Minimize the following function using K-map. $F(A,B,C,D) = \Sigma m (0, 1, 2, 3, 4, 5, 6, 11, 12, 13)$. **(10marks)**

**5)** State and prove De Morgan's theorem for 2 variables. **(6 marks)**

**6)** Simplify the following function using Quine- McCluskey method. $f(a,b,c,d) = \Sigma m (0, 1, 2, 5, 6, 7, 8, 9, 10, 14)$. **(10marks)**

**NOV/DEC 2013**

**1)** Simplify the following Boolean function using Quine-McCluskey method. $F(A,B,C,D,E) = \Sigma m (0, 1, 3, 7, 13, 14, 21, 26, 8) + \Sigma d (2, 5, 9, 11, 17, 24)$. **(16 marks)**

**2)** Simplify the given Boolean function in POS form using k-map and draw the logic diagram using only NOR gates. $F(A,B,C,D) = \Sigma m (0, 1, 4, 7, 8, 10, 12, 15) + \Sigma d (2, 6, 11, 14)$. **(10marks)**

**3)** Convert $78.5_{10}$ into binary. **(3marks)**

**4)** Find the dual and complement of the following Boolean expression, xyz'+x'yz+z(xy+w). **(3marks)**

**APRIL/MAY 2013**

**1)** Reduce the following using Karnaugh map technique: (i) f(A,B,C) = Σm (0, 1, 3, 7) + Σd (2, 5)
(ii) F(w,x,y,z)= Σm (0, 7, 8, 9, 10, 12) + Σd (2, 5, 13). **(16marks)**

**2)** Simplify the following Boolean function using Quine-McCluskey method:
F(A,B,C,D,E,F) = Σm (0, 5, 7, 8, 9, 12, 13, 23, 24, 25, 28, 29, 37, 40, 42, 44, 46, 55, 56, 57, 60, 61).
**(16marks)**

**NOV/DEC 2012**

**1)** Simplify F(A,B,C,D) = Σ (0, 1, 2, 5, 8, 9, 10) in sum of products and product of sums using k-map. **(12marks)**

**2)** Write notes on negative and positive logic. **(4marks)**

**3)** Simplify the expression F(A,B,C,D) = Σ (1, 4, 6, 7, 8, 9, 10, 11,15) using Quine-McCluskey method. **(12marks)**

**4)** Check if NOR operator is associative. **(4marks)**

**NOV/DEC 2011**

**1)** Simplify the following Boolean function F using K-map method:
(i) F(A,B,C,D) = Σ (1, 4, 5, 6, 12, 14, 15) **(4marks)**
(ii) F(A,B,C,D) = Σ (0, 1, 2, 4, 5, 7, 11, 15) **(4marks)**
(iii)F(A,B,C,D) = Σ (2, 3, 10, 11, 12, 13, 14, 15) **(4marks)**
(iv)F(A,B,C,D) = Σ (0, 2, 4, 5, 6, 7, 8, 10, 13, 15) **(4marks)**

**2)** Simplify the following Boolean expression to a minimum number of literals:
(i) $\overline{A}\overline{C}+ABC+A\overline{C}$ **(2 marks)**
(ii) $XYZ+\overline{X}Y+XY\overline{Z}$ **(2 marks)**
(iii)$XY+YZ+X\overline{Y}Z$ **(2 marks)**
(iv)$A\overline{B}+ABD+AB\overline{D}+\overline{ACD}+\overline{A}B\overline{C}$ **(5 marks)**
(v) $BD+BC\overline{D}+A\overline{BCD}$ **(5 marks)**

**APRIL/MAY 2011**

**1)** CONVERT $(1947)_{10}$ into its equivalent octal and hexadecimal representations. **(10 marks)**

**2)** Perform (147-89) using 2's complement binary arithmetic. **(6 marks)**

**3)** Minimize the following expression using k-map.
Y=A'BC'D'+A'BC'D+ABC'D'+AB'C'D+A'B'CD'. **(10 marks)**

**4)** State and prove the De Morgan's theorems. **(6 marks)**

**NOV/DEC 2010**

**1)** Simplify the following 5 variable Boolean expression using McCluskey method.
F = Σm (0, 1, 9, 15, 24, 29, 30) + d (8, 11, 31). **(16 marks)**

**2)** Determine the minterm sum of product form of the switching function. F = Σ (0, 1, 4, 5, 6, 11, 14, 15, 16, 17, 20, 22, 30, 32, 33, 36, 37, 48, 49, 52, 53, 59, 63). **(16 marks)**

**APRIL/MAY 2010**

**1)** Simplify the following using k-map and implement it with two-level NAND gate circuit: F(A,B,C,D) = AB'+ABD+ABD'+A'C'D'+A'BC'. **(16 marks)**

**2)** Simplify the following Boolean function by means of the tabulation method:

**3)** P(A,B,C,D,E,F) = Σ (6, 9, 13, 18, 19, 25, 27, 29, 41, 45, 57, 61) **(12 marks)**

**4)** Simplify xy'+y'z'+x'z' to a minimum number of literals. **(4 marks)**

**NOV/DEC 2009**

**1)** Simplify the following Boolean expression using Quine McCluskey method: F = Σm (0, 9, 15, 24, 29, 30) + d (8, 11, 31). **(16 marks)**

**2)** Implement Boolean expression for EX-OR gate using NAND and NOR gates. **(8marks)**

**3)** Prove that (AB+C+D)(C'+D)(C'+D+E)=ABC+D**.** **(4marks)**

**4)** Using 2's complement perform $(42)_{10} - (68)_{10}$. **(4marks)**

## UNIT – II
## *COMBINATIONAL LOGIC*

**NOV/DEC 2015**

**1)** Design a Full subtractor and derive expression for difference and borrow. Realize using gates. **(16marks)**

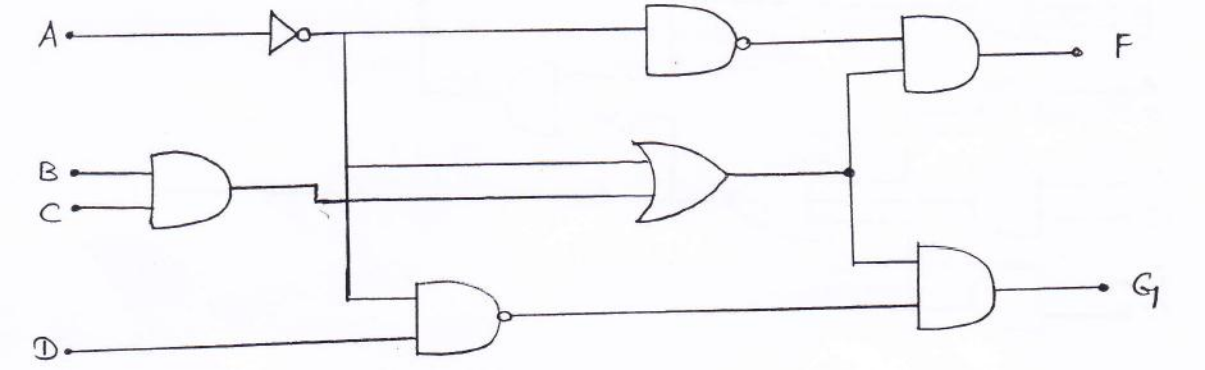
**2)** Design a code converter that converts a 8421 to BCD code. **(16marks)**

**APRIL/MAY 2015**

**1)** Implement the following Boolean function with a multiplexer: F(w,x,y,z) = Σ (2, 3, 5, 6, 11, 14, 15). **(8marks)**

**2)** Construct a 5 to 32 line decoder using 3 to 8 line decoder and 2 to 4 line decoder. **(8marks)**

**3)** Explain the analysis procedure. Analyze the following logic diagram. **(8marks)**




**4)** With neat diagram explain the 4-bit adder with carry look ahead. **(8marks)**

**NOV/DEC 2014**

**1)** Design and implement a 8421 to gray code converter. Realize the converter using only NAND gates. **(16marks)**

**2)** Design 2-bit magnitude comparator and write a Verilog HDL code. **(16marks)**

**APRIL/MAY 2014**

**1)** Design a circuit that converts 8421 BCD code to excess-3 code. **(16marks)**

**2)** Implement the following Boolean function using 8 to 1 multiplexer
F(A,B,C,D) = A'BD'+ACD+B'CD+A'C'D. also implement using 16 to 1 multiplexer. **(16marks)**

**3)** Design a 2-bit magnitude comparator. **(6marks)**

**4)** Design a 2-bit binary multiplier to multiply two binary numbers and produce a 4-bit result. **(10marks)**

**5)** Design a full adder and realize it using only NOR GATES. **(8marks)**

**6)** Design a 4-bit parallel binary adder/subtractor. **(8marks)**

**NOV/DEC 2013**

**1)** Design a combinational circuit to perform BCD addition. **(16marks)**

**2)** Design a 4-bit magnitude comparator with three outputs: A>B, A=B, A<B **(12marks)**

**3)** Construct a 4-bit odd parity generator circuit using gates. **(4marks)**

**APRIL/MAY 2013**

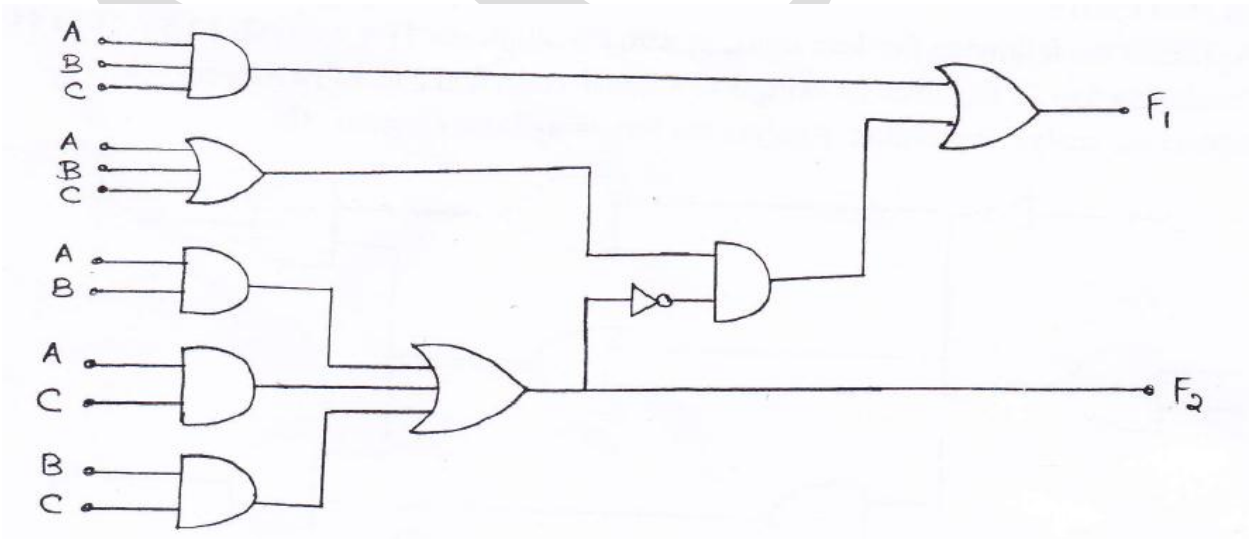
**1)** Design a full adder using two half adders. **(16marks)**

**2)** Design a combinational circuit to convert binary to gray code. **(16marks)**

**3)** Implement the switching function F = Σm (0, 1, 3, 4, 12, 14, 15) using an 8 input MUX. **(16marks)**

**NOV/DEC 2012**

**1)** Analyse the combinational circuit shown in below figure. Determine the truth table and the Boolean expressions governing the outputs of the circuit. **(10marks)**




**2)** Explain BCD adder with a neat block diagram. **(6marks)**

**3)** Design a BCD to excess-3 code converter using logic gates. **(12marks)**

**4)** Draw the diagram of a 4-bit adder subtractor using full adders. **(4marks)**

**5)** Implement F(A,B,C,D) = Σ (1, 3, 4, 11, 12, 13, 14, 15) using 8X1 multiplexer. **(8marks)**

**6)** Design a 4-bit priority encoder. **(6marks)**

**NOV/DEC 2011**

**1)** Write a note on carry propagation. **(8marks)**

**2)** Construct a 5 to 32 line decoder with four 3 to 8 line decoders with enable and a 2 to 4 line decoder. Use block diagrams for components. **(16marks)**

**3)** Implement the following Boolean function with 16x1 multiplexer: F(A,B,C,D) = Σ (0, 1, 3, 4, 8, 9, 15) **(6marks)**

**4)** Write HDL gate level description for 3 to 8 line decoder. **(4marks)**

**APRIL/MAY 2011**

**1)** Design a combinational circuit that comprises only for NOR gates for the following expression giving the input output relation. Y=ABC'+AC+B'C. **(10marks)**

**2)** Draw the schematic of a full adder circuit and give its truth table. **(6marks)**

**3)** Design a BCD to Excess-3 code converter using truth table and k-map simplification. **(10marks)**

**4)** Design a combinational logic using a suitable multiplexer to realize the following Boolean expression. Y=AD'+B'C+BC'D'. **(10marks)**

**5)** Compare and contrast between encoders and multiplexers. **(6marks)**

**NOV/DEC 2010**

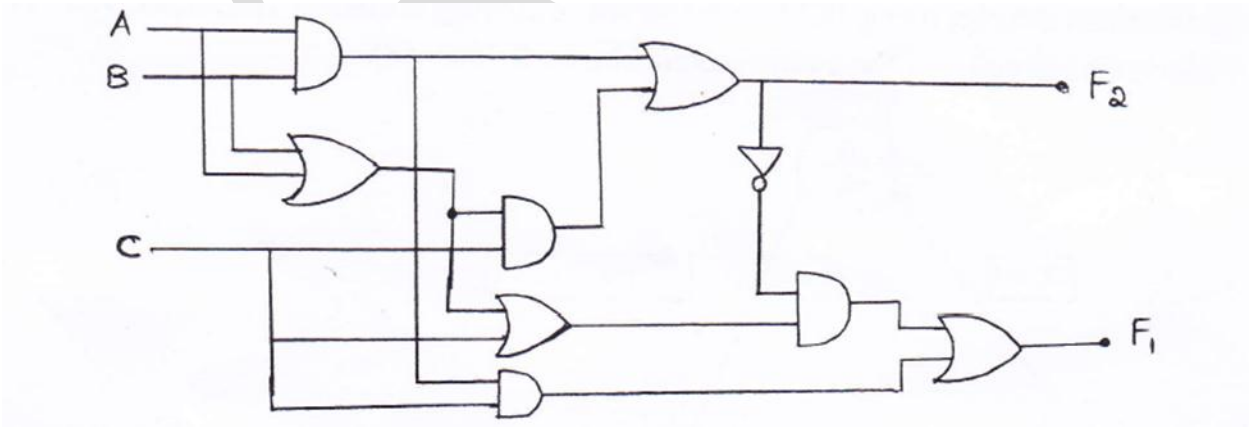
**1)** Relative a BCD to Excess-3 code conversion circuit starting from its truth table. **(16marks)**

**2)** Design a full adder and subtractor using NAND and NOR gates respectively. **(16marks)**

**3)** Implement the following Boolean function using 8:1 MUX. F(A,B,C,D)= ABD+ACD+BCD+ACD. **(16marks)**

**APRIL/MAY 2010**

**1)** Analyse the combinational circuit shown in figure. Find the Boolean functions for the output as a function of the inputs and explain the circuit operation. **(16marks)**




**2)** Implement F(A,B,C)=Σ(1,3,5,6) with a 4:1 multiplexer. **(5marks)**

**3)** Write the HDL code for a 2 to 4 decoder. **(5marks)**

**NOV/DEC 2009**

**1)** Explain the gray code to binary converter with the necessary diagram. **(10marks)**

**2)** Design a half subtractor circuit. **(6marks)**

## *UNIT – III*
## *SYNCHRONOUS SEQUENTIAL LOGIC*

**NOV/DEC 2015**

**1)** Design a sequence detector that detects a sequence of three or more consecutive 1's in a string of bits coming through an input an input line and produces an output whenever this sequence is detected. **(16marks)**

**2)** Design a three bit synchronous counter with T flip flop and draw the diagram. **(16marks)**

**APRIL/MAY 2015**

**1)** A sequential circuit with two D flip flops A and B, one input x and one output z is specified by the following next- state and output equations: A(t+1)= A'+B, B(t+1)=B'x, z=A+B'

(i) Draw the logic diagram of the circuit. **(4marks)**

(ii) Derive the state table. **(3marks)**

(iii)Draw the state diagram of the circuit. **(8marks)**

**2)** Explain the difference between a state table, characteristic table and an excitation table. **(6marks)**

**3)** Consider the Design of a 4-bit BCD counter that counts in the following way: 0000,0001,0010,0011,…..,1001 and back to 0000.

(i) Draw the state diagram. **(4marks)**

(ii) List the next state table. **(4marks)**

(iii)Draw the logic diagram for the circuit. **(8marks)**

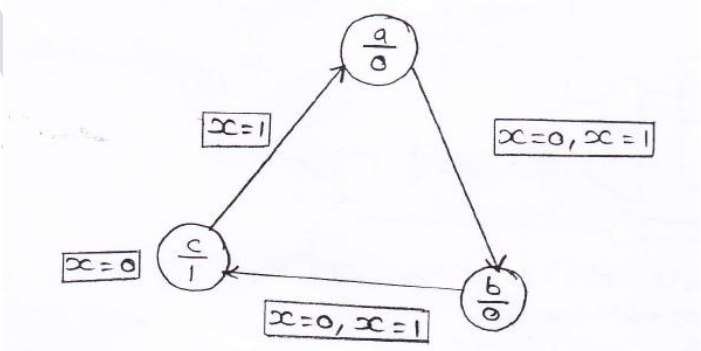
**NOV/DEC 2014**

**1)** Design a MOD-10 synchronous counter using JK flip flops. Write execution table and state table. **(16marks)**

**2)** How race condition can be avoided in a flip flop? **(8marks)**

**3)** Design a synchronous counter using JKFF to count the following sequence 7,4,3,1,5,0,7… **(16marks)**

**4)** Realize the sequential circuit for the state diagram shown below. **(8marks)**



**APRIL/MAY 2014**

**1)** Implement T flip flop using D flip flop and JK flip flop using D flip flop. **(16marks)**
**2)** Design a synchronous counter which counts in the sequence 000,001,010,011,100,101,110,111,000 using DFF. **(16marks)**
**3)** Design a sequence detector to detect the input sequence 101 (overlapping). Use JKFF. **(16marks)**
**4)** Design a 3-bit synchronous up counter using JKFF. **(6marks)**
**5)** Design a 3-bit parallel in serial our shift register and write the HDL code to realize it. **(10marks)**

**APRIL/MAY 2013**

**1)** Using D flip flops design a synchronous counter which counts in the sequence 000,001,010,011,100,101,110,111,000. **(16marks)**
**2)** Design a shift register using JKFF. **(16marks)**

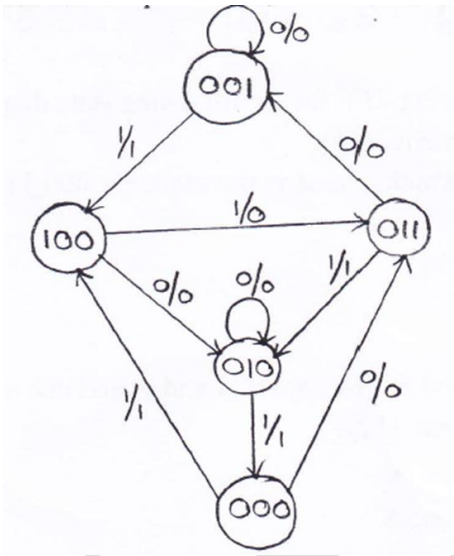
**NOV/DEC 2012**

**1)** Design a 3-bit binary counter. **(10marks)**
**2)** Write the HDL description of TFF and JKFF from DFF and gates. **(6marks)**
**3)** Design a sequential circuit suing RS flip flop for the state table given below using minimum number of flip flops. **(16marks)**

| PRESENT STATE | NEXT STATE | | OUTPUT | |
|---|---|---|---|---|
| | X=0 | X=1 | X=0 | X=1 |
| a | a | b | 0 | 0 |
| b | c | d | 0 | 0 |
| c | a | d | 0 | 0 |
| d | e | f | 0 | 1 |
| e | a | f | 0 | 1 |
| f | g | f | 0 | 1 |
| g | a | f | 0 | 1 |

**NOV/DEC 2013**

**1)** Design a synchronous counter with the following sequence: 0, 1, 3, 7, 6, 4 and repeats. Use JKFF. **(16marks)**
**2)** Design the sequential circuit specified by the following state diagram using TFF. **(16marks)**




**NOV/DEC 2011**

**1)** Design a MOD 16 up counter using JKFF. **(16marks)**

**2)** With suitable example explain state reduction and state assignment**.** **(16marks)**

**APRIL/MAY 2011**

**1)** Design a synchronous counter using JK flip flops to count the following sequence. "1-3-15-5-8-2-0-12-6-9". **(16marks)**

**2)** A synchronous counter with four JKFF has the following connections: **(16marks)**
$J_A=K_A=1$; $J_B=Q_AQ_{D'}$, $K_A=Q_A$ ; $J_C=K_C=Q_AQ_B$ ; $J_D=Q_AQ_BQ_C$ and $K_D=Q_A$

**NOV/DEC 2010**

**1)** Design a clocked sequential machine using TFF for the following state diagram. Use state reduction if possible. Also use straight state assignment. **(16marks)**

**2)** Using RSFF design a parallel counter which counts in the sequence 000,111,101,110,001,010,000. **(16marks)**

**3)** Design a T flip flop from logic gates. **(16marks)**

**APRIL/MAY 2010**

**1)** A sequential circuit with two DFF, A and B: two inputs, x and y: and one output z, is specified by the following next state and output equations: **(12marks)**

**A(t+1) = x'y+xA**
**B(t+1) = x'B+xA**
**Z = B**

Draw the logic diagram of the circuit, derive the state table and derive the state diagram.

**2)** How do ripple counters differ from synchronous counter? Explain. **(4marks)**

**3)** Explain how shift registers are used in serial addition with a neat diagram. **(8marks)**

**4)** Give the HDL description of master slave JK flip flop. **(8marks)**

**5)** Design a sequential circuit using RSFF for the state table given below using minimum number of flip flops. **(10marks)**

| PRESENT STATE | NEXT STATE | | OUTPUT | |
|---|---|---|---|---|
| | X=0 | X=1 | X=0 | X=1 |
| a | a | b | 0 | 0 |
| b | c | d | 0 | 0 |
| c | a | d | 0 | 0 |
| d | e | f | 0 | 1 |
| e | a | f | 0 | 1 |
| f | g | f | 0 | 1 |
| g | a | f | 0 | 1 |

**NOV/DEC 2009**

**1)** Design and implement a MOD 5 synchronous counter using JKFF. **(16marks)**

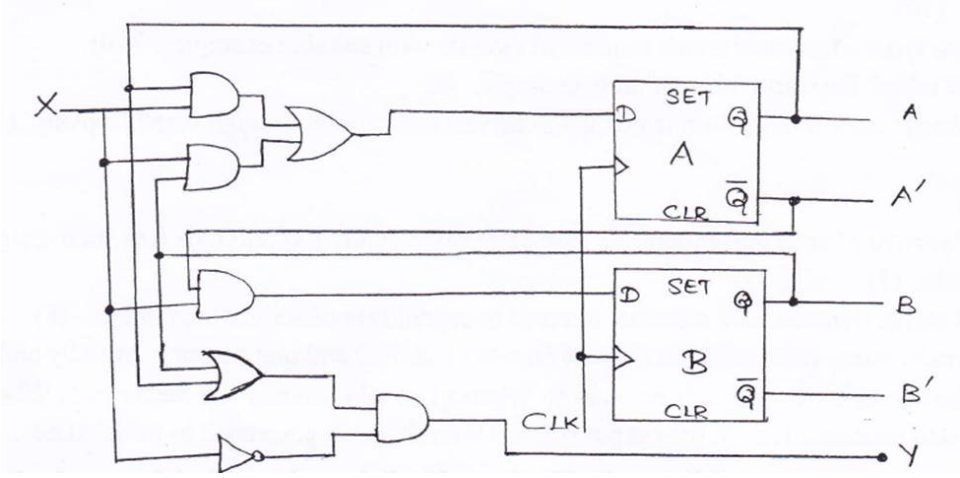
**2)** Explain the working of master slave JKFF. **(10marks)**

**3)** Draw the diagram for a 3-bit ripple counter. **(6marks)**

## *UNIT – IV*
## *ASYNCHRONOUS SEQUENTIAL CIRCUIT*

**NOV/DEC 2015**

**1)** Analyze the following clocked sequential circuit and obtain the state equations and state diagram. **(16marks)**




**2)** Design a serial adder using a full adder and a flip flop. **(16marks)**

**APRIL/MAY 2015**

**1)** Explain the Race-free state assignment procedure. **(8marks)**

**2)** Reduce the number of states in the following state diagram. Tabulate the reduced state table and draw the reduced state diagram**.** **(8marks)**

| PRESENT STATE | NEXT STATE | | OUTPUT | |
|---|---|---|---|---|
| | X=0 | X=1 | X=0 | X=1 |
| a | a | b | 0 | 0 |
| b | c | d | 0 | 0 |
| c | a | d | 0 | 0 |
| d | e | f | 0 | 1 |
| e | a | f | 0 | 1 |
| f | g | f | 0 | 1 |
| g | a | f | 0 | 1 |

**3)** Explain the hazards in combinational circuit and sequential circuit and also demonstrate a hazard and its removal with example. **(16marks)**

**NOV/DEC 2014**

**1)** An asynchronous sequential circuit is described by the following excitation and output function. $Y=x_1x_2+(x_1+x_2)y$, $Z=Y$. **(16marks)**

(i) Draw the logic diagram of the circuit.

(ii) Derive the transition table and output map.

(iii)Describe the behaviour of the circuit.

**APRIL/MAY 2014**

**1)** Explain the steps for the design of asynchronous sequential circuits**.** **(16marks)**

**2)** Implement the switching function $F = \Sigma m (1, 3, 5, 7, 8, 9, 14, 15)$ by a static hazard free two level AND- OR gate network. **(16marks)**

**3)** Explain the two types of asynchronous sequential circuits with suitable examples. **(10marks)**

**4)** What is a flow table? Explain with a suitable example. **(6marks)**

**5)** What is an hazard? How to remove hazards using hazard covers in Karnaugh map? Explain. **(10marks)**

**NOV/DEC 2013**

**1)** What is the objective of state assignment in asynchronous circuit? Explain race free state assignment with an example. **(8marks)**

**2)** Discuss about static, dynamic and essential hazards in asynchronous sequential circuits. **(8marks)**

**3)** Design an asynchronous sequential circuit with inputs $x_1$ and $x_2$ and one output z. initially and at any time if both the inputs are 0, output is equal to 0. When $x_1$ or $x_2$ becomes 1, z becomes 1. When second input also becomes 1, z=0; the output stays at 0 until circuit goes back to initial state… **(16marks)**

**APRIL/MAY 2013**

**1)** Explain the types of hazards in digital circuits. **(8marks)**

**2)** Implement the switching function $F = \Sigma m (1, 3, 5, 7, 8, 9, 14, 15)$ by a static hazard free 2 level AND-OR gate network. **(8marks)**

**3)** Explain the steps for the design of asynchronous sequential circuits. **(16marks)**

**NOV/DEC 2012**

**1)** Explain race-free state assignment with an example. **(16marks)**

**2)** Write detailed notes on hazards in combinational circuits and sequential circuits. **(16marks)**

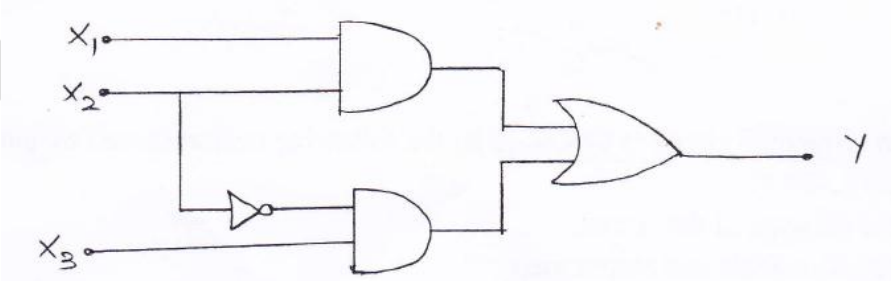
**NOV/DEC 2011**

**1)** With suitable example explain state reduction and state assignment**.** **(16marks)**

**2)** Write a detailed note on race free state assignment. **(16marks)**

**APRIL/MAY 2011**

**1)** Determine whether the following circuit has a static hazard or not. If yes design a hazard-free logic for the same input and output relation. **(6marks)**




**NOV/DEC 2010**

**1)** Find a static and dynamic hazard free realization for the following function using (i) NAND gates. (ii) NOR gates. $F(a,b,c,d) = \Sigma m (1, 5, 7, 14, 15)$. **(16marks)**

**APRIL/MAY 2010**

**1)** Discuss in detail different types of hazards in digital circuits. **(12marks)**

**2)** Draw the block diagram of an asynchronous sequential circuit. List the steps involved in the design of an asynchronous sequential circuit. **(6marks)**

## *UNIT – V*
## *MEMORY AND PROGRAMMABLE LOGIC*

**APRIL/MAY 2015**

**1)** Implement the following two Boolean functions with a PLA. $F_1$=AB'+AC+A'BC', $F_2$=(AC+BC)' **(10marks)**

**2)** Give the internal block diagram of 4×4 RAM. **(6marks)**

**NOV/DEC 2014**

**1)** Design a BCD to Excess-3 code converter and implement using suitable PLA. **(16marks)**

**2)** Discuss on the concept of working and applications of semiconductor memories. **(16marks)**

**APRIL/MAY 2014**

**1)** Implement the following functions using PLA. A(x, y, z) = Σm (1, 2, 4, 6), B(x,y,z) = Σm (0, 1, 6, 7), C(x, y, z) = Σm (2, 6). **(16marks)**

**2)** The following messages have been coded in the even parity hamming code and transmitted through a noisy channel. Decode the messages, assuming that at most a single error has occurred in each codeword. (i) 1001001 (ii) 0111001 (iii) 1110110 (iv) 0011011. **(16marks)**

**NOV/DEC 2013**

**1)** Implement the following two Boolean functions using PLA with 3 inputs, 4 product terms and 2 outputs. $F_1$ = Σm (3, 5, 6, 7), $F_2$ = Σm (1, 2, 3, 4). **(16marks)**

**2)** Implement the two following Boolean functions using a 8×2 PROM.
$F_1$ = Σm (3, 5, 6, 7) $F_2$ = Σm (1, 2, 3, 4). (**6marks)**

**NOV/DEC 2012**

**1)** Write notes on PLA and PAL. **(8marks)**

**2)** Write notes on RAM, its operation and its types. **(10marks)**

**NOV/DEC 2010**

**1)** Implement the switching functions $Z_1$=ABDE+ABCDE+BC+DE, $Z_2$=ACE, $Z_3$=BC+DE+CDE+BD, $Z_4$= ACE+CE using 5×8×4 PLA. **(16marks)**

**APRIL/MAY 2010**

**1)** Design a combinational circuit defined by the following Boolean functions using a PAL: **(16marks)**
W(A,B,C,D) = Σ (2, 12, 13), X(A,B,C,D) = Σ (7, 8, 9, 10, 11, 12, 13, 14, 15),
Y(A,B,C,D) = Σ (0, 2, 3, 4, 5, 6, 7, 8, 10, 11, 15), Z(A,B,C,D) = Σ (1, 2, 8, 12, 13)

**2)** Write notes on the different types of ROM. **(6marks)**

**NOV/DEC 2009**

**1)** Write the comparison between PROM, PLA, PAL**.** **(8marks)**

**2)** Design a BCD to Excess-3 code converter and implement using PLA. **(10marks)**

***Prepared by,***

***V.Lavanya, AP/ECE***