



AKSHEYAA COLLEGE OF ENGINEERING

Puludivakkam, (Near Nelvay Junction), Maduranthagam Taluk,
Kancheepuram 603 314, Tamil Nadu, India.
Phone: + 91 44 27568004-02-05, email: principal@ace.ac.in
(An ISO 9001:2008 Certified Institution)



Department of Electronics & Communication Engineering

Year/Sem: II/III

EC6302: Digital Electronics

Unit - I: Minimization Techniques and Logic Gates

Part A: Two Mark Questions

1. State De Morgan's theorem. (May/June 2013)
2. What are Don't care terms? (May/June 2013)
3. State Distributive law. (Nov/Dec 2013)
4. What is Prime Implicant? (Nov/Dec 2013)
5. Apply De-Morgan's theorem to $[(A+B)+C]'$. (May/June 2014)
6. Convert 0.35 to equivalent hexadecimal number. (May/June 2014)
7. Simplify the following Boolean expression into one literal $W'X(Z'+YZ)+X(W+Y'Z)$. (Nov/Dec 2014)
8. Draw the CMOS inverter circuit. (Nov/Dec 2014)
9. Simplify: $AB'C+A'B'C$. (Nov/Dec 2014)
10. Write the truth table for EXOR gate. (Nov/Dec 2014)
11. Define 'min term' and 'ax term'. (Apr/May 2015)
12. Write a note on tristate gates. (Apr/May 2015)
13. State the advantages of CMOS logic. (Apr/May 2015)
14. Convert $Y=A+BC'+AB+A'BC$ into canonical form. (Apr/May 2015)

Part B: Sixteen Mark Questions

1. Minimize the given switching function using Quine McClusky method. $f(x_1,x_2,x_3,x_4)=\sum m(0,5,7,8,9,10,11,14,15)$. (16) (May/June 13)
2. Simplify the given Boolean function into (i) sum of products form (ii) product of sum form and implement using basic gates. $F(A,B,C,D)=\sum(0,1,2,5,8,9,10)$. (16) (May/June 13)
3. (i) Simplify $xy+x'z+yz$. (6) (Nov/Dec 2013)
(ii) Simplify the following expression using K-map method. $Y=\sum m(7,9,10,11,12,13,14,15)$. (10) (Nov/Dec 2013)
4. Simplify the following function using tabulation method $Y(A,B,C,D)=\sum m(0,1,2,5,6,7,8,9,10,14)$ and implement using only NAND gates. (16) (May/June 14)
5. (i) Given $Y(A,B,C,D)=\prod M(0,1,3,5,6,7,10,14,15)$, draw the K-map and obtain the simplified expression. Realize the minimum expression using basic gates. (8) (May/June 14)

- (ii) Implement the expression $Y(A,B,C)=\Pi M(0,2,4,5,6)$ using only NOR-NOR logic. (4) (May/Jun 14)
- (iii) Implement EXOR gate using only NAND gates. (4) (May/Jun 14)
15. (i) Convert the following function into product of maxterms. $F(A,B,C)=(A+B')(B+C)(A+C')$. (4) (Nov/Dec 2014)
- (ii) Using Quine McClusky method, simplify the given function. $F(A,B,C,D)=\sum m(0,2,3,5,7,9,11,13,14)$. (12) (Nov/Dec 2014)
16. Draw the multiple level two input NAND circuit for the following expression: $F=(AB'+CD')E+BC(A+B)$. (4) (Nov/Dec 2014)
17. Simplify the Boolean function $F=\Pi(1,3,5,6,7,10,14,15)$ and realize using NAND gates only. (10) (Nov/Dec 2014)
18. (i) Using tabulation method minimize the following function $F=\sum(0,1,2,8,9,15,17,21,24,25,27,31)$. (10) (Nov/Dec 2014)
- (ii) Simplify the expression $Y=AB+AB' \cdot (A'C)'$. (6) (Nov/Dec 2014)
19. Simplify using Quine McCluskey method and verify your result using K-map $F=\sum(0,1,2,5,7,8,9,10,13,15)$. (16) (Apr/May 2015)
20. (i) Express the Boolean functions $F=A+B'C$ in a sum of minterms. (10) (Apr/May 2015)
- (ii) Simplify the following Boolean expression using Boolean algebra. (1) $x'y'z+x'yz+xy'$. (2) $xyz+x'z+yz$. (6) (Apr/May 2015)
21. (i) Simplify $T(x,y,z)=(x+y)[x'(y'+z)]'+x'y'+x'z'$. (6) (Apr/May 2015)
- (ii) Simplify the Boolean function and draw the logic diagram $f(w,x,y,z)=\sum(0,1,2,4,5,6,8,9,12,13,14)$. (10) (Apr/May 2015)
22. (i) Realize AND, OR and NOT gates using NAND gate. (6) (Apr/May 2015)
- (ii) Using tabulation method simplify $F(A,B,C,D,E)=\sum(0,1,4,5,16,17,21,25,29)$. (10) (Apr/May 2015)

Unit - II: Combinational Circuits

Part A: Two Mark Questions

1. Differentiate a decoder from a demultiplexer. (Apr/May 2015)
2. Design a half-subtractor combinational circuit to produce the outputs Difference and Borrow. (May/Jun 2013) & (Nov/Dec 2014)
3. List few applications of Multiplexer. (Nov/Dec 2013)
4. Draw the logic diagram of a 4 line to 1 line Multiplexer. (May/Jun 2013)
5. Draw the logic circuit of a 2bit comparator. (May/Jun 2014) & (Apr/May 2015)
6. Construct 4-bit parallel adder/subtractor using Full adders and XOR gates. (Nov/Dec 2014)
7. Convert a two-to-four line decoder with enable input to 1x4 demultiplexer. (Nov/Dec 2014)
8. State the function of select inputs of a MUX. (Nov/Dec 2014)
9. Give the logic expressions for sum and carry in full adder circuit. (Apr/May 2015)

10. Enumerate some of the combinational circuits. (Nov/Dec 2013) & (Apr/May 2015)
11. What is priority encoder? (May/Jun 2014)

Part B: Sixteen Mark Questions

1. Design a BCD adder and explain its working with necessary circuit diagram. (16) (May/Jun 2013), (Nov/Dec 2014) & (Apr/May 2015)
2. Design a 4 bit magnitude comparator and draw the circuit. (16) (May/Jun 2013), (Nov/Dec 2013), (Nov/Dec 2014) & (Apr/May 2015)
3. Draw the logic diagram of BCD - decimal decoder and explain its operations. (16) (Nov/Dec 2013) & (Nov/Dec 2014)
4. Design a binary to gray code converter. (8) (May/Jun 2014)
5. (i) Design a full subtractor using demultiplexer. (8) (May/Jun 2014) & (Nov/Dec 2014)
(ii) Explain the working of carry look ahead adder. (8) (May/Jun 2014) & (Apr/May 2015)
6. Implement the function using multiplexer $F = \sum(0,1,3,4,8,9,15)$. (8) (Nov/Dec 2014) & (Apr/May 2015)
7. Design a combinational circuit that converts 4 bit Gray Code to a 4 bit binary number. Implement the circuit. (16) (Apr/May 2015)
8. (i) Draw the logic diagram of Binary to octal decoder and explain the working in detail. (8) (May/Jun 2014) & (Apr/May 2015)
(ii) Design a 4*1 multiplexer circuit. (8) (Apr/May 2015)

Unit - III: Sequential Circuits

Part A: Two Mark Questions

1. How many flip-flops are required to build a binary counter that counts from 0 to 1023? (May/Jun 2013)
2. How a D flip-flop is converted into T flip-flop. (May/Jun 2013)
3. Define: Latches. (Nov/Dec 2013)
4. Write short notes on Digital Clock. (Nov/Dec 2013)
5. Compare the logics of synchronous counter and ripple counter. (May/Jun 2014) & (Nov/Dec 2014)
6. Sketch the logic diagram of a clocked SR flip-flop. (May/Jun 2014)
7. Realize JK flip-flops. (Nov/Dec 2014)
8. Mention the advantage of JK-FF over SR-FF. (Nov/Dec 2014)
9. Draw the basic block diagram of sequential circuits. (Nov/Dec 2014)
10. Draw the circuit diagram of a 3bit Ring counter. (Apr/May 2015)
11. Draw the truth table of RS flip-flop. (Apr/May 2015)
12. What is the minimum no. of flip flop needed to design a counter of modulus 60? (Apr/May 2015)
13. Realize T-FF from JK-FF. (Apr/May 2015)

Part B: Sixteen Mark Questions

1. Design a counter to count the sequence 0,1,2,4,5,6 using SR FFs. (16) (May/Jun 2013)
2. Design a 4 bit Asynchronous Ripple counter and explain its operation with timing diagrams. (May/Jun 2013)
3. (i) Draw the block diagram of SR – FF and explain. (6) (Nov/Dec 2013)
(ii) Explain about triggering of flip-flops. (10) (Nov/Dec 2013) & (Nov/Dec 2014)
4. Draw the block schematic of up-down counter and explain its operation. (16) (Nov/Dec 2013) & (Apr/May 2015)
5. Design the sequential circuit that has 3 flip-flops A, B, and C, one input x and one output y. the circuit is to be designed by treating the unused states as don't care conditions. Use JK flip-flops in the design. State diagram of the circuit is given as below. (16) (May/Jun 2014) & (Nov/Dec 2014)
6. (i) Design a 3bit synchronous counter using JK flip flops. (12) (Nov/Dec 2014)
(ii) Explain the differences between a state table, a characteristic table and an excitation table. (4) (Nov/Dec 2014)
7. Design a synchronous MOD 12 counter using FFs. (10) (Nov/Dec 2014)
8. (i) Explain how to convert serial data to parallel and parallel data to serial using shift registers. (10) (Nov/Dec 2014)
(ii) Realize D and T FF using JK FF. (6) (Nov/Dec 2014)
9. Describe JK-FF with its characteristic table & characteristic equation. (6) (Apr/May 2015)
10. Using D flip-flops design a synchronous counter which counts in the sequence. 000, 001, 010, 011, 100, 101, 110, 111, 000. (16) (Apr/May 2015)
11. Design a sequential circuit with two D FFs A and B and one input x. when $x=0$, the state of the circuit remains the same. When $x=1$, the circuit goes through the state transitions from 00-01-11-10-11-01... (16) (Apr/May 2015)

Unit - IV: Memory Devices

Part A: Two Mark Questions

1. Compare and contrast static RAM and dynamic RAM. (Apr/May 2015)
2. What is difference between PAL and PLA? (May/Jun 2013)
3. What are the different types of programmable logic devices? (May/Jun 2013) & (Nov/Dec 2014)
4. What is Volatile and Non-Volatile memory? (Nov/Dec 2013)
5. Give the advantages of RAM. (Nov/Dec 2013)
6. Draw the structure of a static RAM cell. (May/Jun 2014)
7. List the advantages of PLDs. (May/Jun 2014)
8. Compare and contrast EEPROM and flash memory. (Nov/Dec 2014)
9. What is a Field programmable Gate Arrays (FPGA) device? (Nov/Dec 2014)
10. How many address lines are required for a 4K ROM? (Nov/Dec 2014)
11. $Y=AB'+A'$. Implement using ROM. (Apr/May 2015)

12. What is the basic difference between the RAM & ROM circuitry? (Apr/May 2015)

Part B: Sixteen Mark Questions

- Design using PAL the following Boolean functions.
 $W(A,B,C,D) = \sum(2,12,13)$.
 $X(A,B,C,D) = \sum(7,8,9,10,11,12,13,14,15)$.
 $Y(A,B,C,D) = \sum(0,2,3,4,5,6,7,8,10,11,15)$.
 $Z(A,B,C,D) = \sum(1,2,8,12,13)$. (16) (May/Jun 2013)
- Design and explain a 32x8 ROM. (16) (May/Jun 2013)
- Discuss in detail about the classifications of memories. (16) (Nov/Dec 2013) & (Apr/May 2015)
- Discuss in detail about the FPGA with suitable diagrams. (16) (Nov/Dec 2013), (Nov/Dec 2014) & (Apr/May 2015)
- (i) Explain the read cycle and write cycle timing parameters of a RAM with the help of timing diagram. (8) (May/Jun 2014), (Nov/Dec 2014) & (Apr/May 2015)
(ii) Draw the dynamic RAM cell and explain its operation. (8) (May/Jun 2014) & (Apr/May 2015)
- Design a BCD to Excess-3 code converter using PLA. (16) (May/Jun 2014)
- (i) Write short notes on EAPROM and static RAM cell using MOSFET. (6) (Nov/Dec 2014)
(ii) Using eight 64x8 ROM chips with an enable input and a decoder, construct a 512x8 ROM. (10) (Nov/Dec 2014)
- Use PLA with 3 inputs, 4 AND terms and two outputs to implement the following two Boolean functions. $F_1(A,B,C) = \sum m(3,5,6,7)$ and $F_2(A,B,C) = \sum m(1,2,3,4)$ (12) (Nov/Dec 2014)
- (i) Derive the PLA programming table for the combinational circuit that squares a 3 bit number. Minimize the number of product terms. (10) (Nov/Dec 2014)
(ii) Differentiate between (1) Static and dynamic memory (2) Primary memory and secondary memory. (6) (Nov/Dec 2014)
- Explain the structure of PAL and PLA, how a combinational logic function is implemented in PAL and PLA? Explain with example for each. (16) (Apr/May 2015)
- Explain memory decoding. Compare the RAM, ROM, PROM & EPROM. (8) (Apr/May 2015)

Unit - V: Synchronous and Asynchronous Sequential Circuits

Part A: Two Mark Questions

- What are hazards? (May/Jun 2013) & (Nov/Dec 2013)
- Compare the ASM chart with a conventional flow chart. (May/Jun 2013) & (Apr/May 2015)
- Define ASM chart. What are the basic building blocks of a Algorithmic state machine chart? (Nov/Dec 2014)
- What is synchronous sequential circuit? (Nov/Dec 2013)

5. What is a state diagram? Give an example. (May/Jun 2014)
6. What is critical race condition in asynchronous sequential circuits? Give an example. (Nov/Dec 2014)
7. Differentiate between static and dynamic hazards. (Nov/Dec 2014)
8. List the problems that arise in asynchronous circuits. (Apr/May 2015)
9. What is the most important consideration in making state assignments for asynchronous network? (Apr/May 2015)
10. Distinguish between a combinational logic circuit and a sequential logic circuit. (Apr/May 2015)

Part B: Sixteen Mark Questions

1. Design a hazard free asynchronous circuit that changes state whenever the input goes from logic 1 to logic 0. (16) (May/Jun 2013)
2. Design a serial binary adder using delay flip-flop. (16) (Nov/Dec 2013)
3. List out various problems arise in asynchronous circuits. Explain any two problems in detail. (16) (Nov/Dec 2013)
4. Design a T flip-flop using logic gates. Derive the state table, state table, state diagram, primitive flow table and transition table and merger graph. Draw the logic circuit. (16) (May/Jun 2014)
5. Design an asynchronous sequential circuit that has 2 input's x_1 and x_2 and one output z . When $x_1=0$, output is 0. The change in x_2 that occurs while x_1 is 1 will cause output $z=1$. The output z will remain 1 until x_1 returns to 0. (16) (May/Jun 2014)
6. Design an asynchronous sequential circuit with inputs A and B and an output Y. initially and at any time if both the inputs are 0, the output, Y is equal to 0. When A or B becomes 1, Y becomes 1. When the other input also becomes 1, Y becomes 0. The output stays at 0 until circuit goes back to initial state. (16) (Nov/Dec 2014)
7. (i) What is a hazard in an asynchronous sequential circuits? Define static hazard, dynamic hazard and essential hazard. (8) (Nov/Dec 2014)
(ii) What is the significance of state assignment? Explain the different techniques used for state assignment. (8) (Nov/Dec 2014)
8. Design a sequence detector to detect the sequence 101 from 10101. (16) (May/Jun 2014) & (Nov/Dec 2014)
9. With ASM chart design a binary multiplier. (16) (Apr/May 2015)
10. Explain the different types of hazards. Design a hazard free circuit for $y=x_1x_2+x_2'x_3$. (16) (Apr/May 2015)
11. Explain how a state graph for a sequential machine can be converted to an equivalent ASM chart. (8) (May/Jun 2013) & (Apr/May 2015)
12. Design a sequential detector that receives a stream of input bits. The circuit should recognize the pattern 010 and produce an output whenever this pattern is received. (16) (Apr/May 2015)